



# Smart Stacking™

## A Wafer-stacking Technology Platform

May 2009

By Dr. Bernard Aspar, Vice President Tracit BU, Dr. Ian Cayrefourcq, Director Technology Applications and Dr. Jocelyne Wasselin, VP Business Development  
**Soitec**

### A Solution Driven by an Industry in Transition

As IDMs and foundries grapple with traditional 2D scaling and the exponentially increasing complexity, time and investment necessary to develop next generation process nodes, microelectronics technology is moving into the third dimension. Although 3D architectural concepts have been on the industry's radar for decades, adoption is only now growing thanks to recent advances in stacking technologies. 3D vertical scaling improves density and performance, and also offers "more-than-Moore" benefits through the ability to combine disparate technologies into a single chip. The combination of these factors is pushing 3D integration onto the Moore's Law scaling path.

Marketplace demands are also pulling 3D integration into the mainstream. Responding to strong consumer appetites for ultra-compact form factor, multifunction electronic devices, consumer product manufacturers are employing proven multi-die stack and early stage 3D technologies to create products that are smaller, thinner and lighter in weight than competitive offerings. Many medical, military and aerospace applications also have similar smallest size requirements, and the question of whether or not to use stacking has vanished. Now the challenge is to choose from among multiple implementation options according to criteria of costs, risks and resulting power consumption, performance and reliability.

The global passion for "greener", more power-efficient electronic products and systems is also driving 3D integration as designers seek to capture every available power-saving and power-efficient performance improvement. Integrating slower, power-hungry chip-to-chip interconnections and bringing them on-chip can produce order-of-magnitude efficiency gains per net. Further benefits are realized from reduction in length of on-chip signalling paths by using the 3<sup>rd</sup> dimension to reduce routed distance between connected devices. These 3D benefits compensate for efficiency losses coming from the rising effective resistance of copper interconnects accompanying recent node scaling, and also give longer useful design life to more mature nodes.

While stacked die-to-die assembly approaches to multi-chip integration have seen commercial use in various applications, recent advances in wafer-level stacking offer a more compelling approach to 3D integration in terms of overall density, performance, manufacturing cycle time, power savings, finished stack height, reliability and cost. While the benefits are application dependent, wafer-scale approaches are especially compelling for smaller die sizes. Almost all existing chips can be converted to a wafer-level stacking approach.

Additionally, use of the 3<sup>rd</sup> dimension enables new chip structures, with the ability to transfer finished circuits onto a new handle wafer, the opportunity to expose the backside of devices, and the full realization of 3D multi-wafer stacking.

3D interconnects use through-silicon vias (TSVs), to make electrical connections between active layers and to the external world. TSV size

(cross sectional area and length) determines 3D interconnect density and cost. The enabling technology for maximizing TSV density is a stacking technology that produces very thin layers which allow reductions in the size and cost of TSVs.

The Smart Stacking technology platform from the Soitec Group satisfies each of these market drivers, by enabling new chip architectures and the stacking of the very thin layers needed to manufacture the most compact form factor and highest TSV interconnect density implementations.

## What is Smart Stacking™?

Soitec Group publicly announced its Smart Stacking technology platform for wafer-to-wafer integration in March, 2009. Comprised of low-temperature (below 400°C), high-energy molecular wafer bonding, surface conditioning and thinning technologies, the Smart Stacking platform scales from 150mm to 300mm wafer diameters and adapts to a range of starting materials. It was developed by a team with a track record of industrialization success in combining pioneering materials research with high-volume production know-how from both the silicon wafer and microelectronics manufacturing industries. The Smart Stacking technology is available from Soitec as a production service and as a licensable, transferable technology.

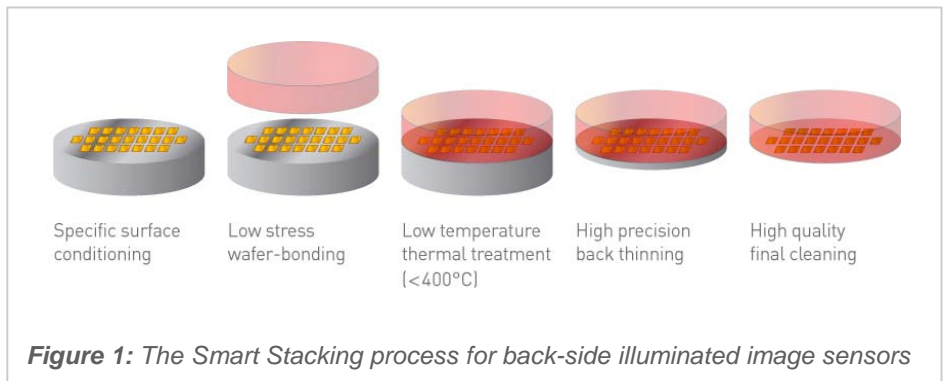


Figure 1: The Smart Stacking process for back-side illuminated image sensors

The Smart Stacking technology provides the ability to transfer very thin layers in a high throughput manufacturing environment. Thinner layers allow for smaller TSVs which enable smaller die sizes for higher interconnect densities making the Smart Stacking technology well-suited for high volume applications. The Smart Stacking technology platform is compatible with alignment techniques at +/- 1µm.

Stacking processed or semi-processed wafers significantly reduces the thermal budget available for bonding, so Smart Stacking utilizes surface preparation know-how and low temperature oxide-oxide molecular bonding technology, with special processes to control and increase the bonding energy within a reduced thermal window (see Figure 2). By avoiding adhesive or thermo-compressive bonding techniques, stress to devices and interconnects and wafer deformation are minimized, thereby increasing yields and reliability.

Through many years of SOI substrate manufacturing Soitec has developed expertise in surface preparation, cleaning and high-precision planarization techniques which contribute significant value in Smart Stacking applications. These include: the ability to control nanometer-scale roughness; the ability to develop process steps to maintain edge quality (see Figure 3a); and the ability to bond dissimilar surfaces. Thanks to cleaning technology know-

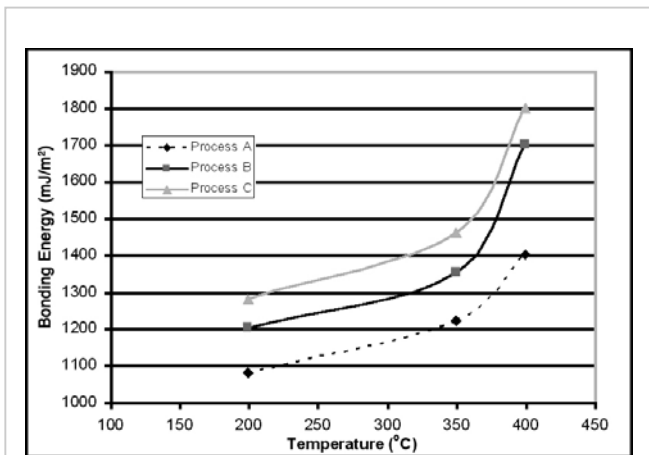


Figure 2: Bonding energy optimization at low temperature comparing multiple Smart Stacking options

how Soitec can deliver stacked wafers suitable for re-entry into a semiconductor fabrication line for post-processing.

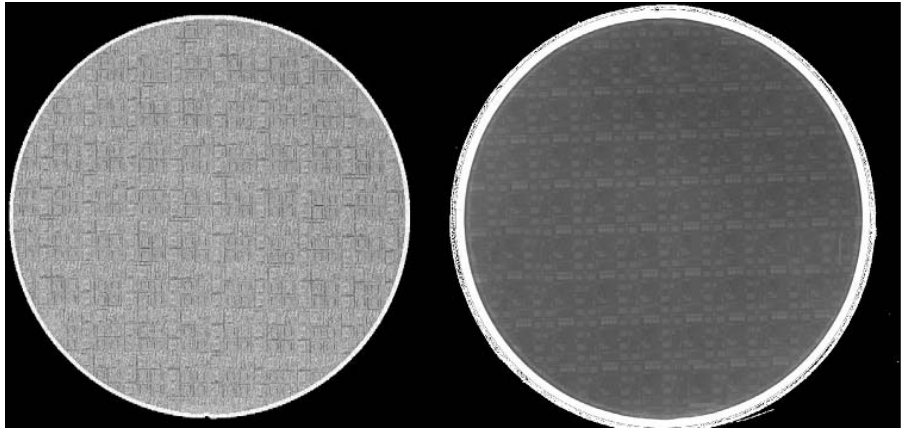
The Smart Stacking technology platform combines wafer thinning techniques such as high precision grinding, and chemical and mechanical thinning with controlled uniformity. These thinning processes can achieve a 10µm thickness for a bulk donor wafer, but when combined with the etch stop layer of an SOI wafer they can achieve thicknesses less than 100nm with a uniformity of +/-75Å. The Smart Stacking thinning techniques are now being commercially used to build back-side-illuminated (BSI) image sensors by transferring layers a few µm thick onto a silicon handle wafer. This technology is compliant with military reliability standard MIL-STD-883 (see *Figure 3b*).

## Smart Stacking Rooted in Proven Industry Enabling Technologies

For nearly two decades Soitec has been applying its Smart Cut™ technology to mass produce SOI (silicon-on-insulator) substrates that meet or exceed semiconductor industry requirements. Through innovation, in response to changing market demands and by a process of continuous improvement, progress has been driven along two vectors: extending manufacturing capabilities to satisfy challenging technical requirements of nanotechnologies (such as the 32nm CMOS node), and reducing SOI manufacturing cost to allow consumer applications to profit from SOI performance, circuit isolation and energy efficiency. Today, Soitec fabricates SOI wafers in high volume characterized by an overall quality identical to bulk silicon wafers, with an SOI thickness control ranging from 100nm for lowest cost processing to 1nm (2 atomic layers) for technically advanced products.

Smart Cut technology involves wafer cleaving technology from which it derives its name; as well as surface preparation, wafer bonding, thinning and finishing. These technology building blocks have been successfully applied to produce a wide variety of semiconductors used in PCs, popular gaming platforms, wireless and wired communication equipment, cameras, supercomputers, automobiles and aerospace vehicles.

Since its 2006 acquisition of Tracit Technologies, Soitec has also assimilated complementary bonding and thinning technologies developed specifically for wafer-level circuit stacking.



**Figure 3a:** Acoustic microscopy of bonded wafers showing edge treatment impact

Test	Condition	Pass/Fail
Operating life test (endurance)	125°C/2000h	✓
High temperature storage	150°C/1000h	✓
Temperature cycling	-55°C, +125°C, 15°/min	✓
Moisture resistance	65°C, -10°C, 90-100% RH- 10 days	✓

**Figure 3b:** Reliability results for BSI image sensors. Also passed Vibration, Mechanical Shock and Pull test (Courtesy of e2v)

## Smart Stacking™ Application Examples

The Smart Stacking technology allows separately processed wafers to be integrated together into a single chip, as in the example of photonic devices fabricated on an SOI substrate being transferred onto a bulk CMOS logic wafer. The end result shown in *Figure 4* is a high speed communications controller with on-chip optical transceivers.

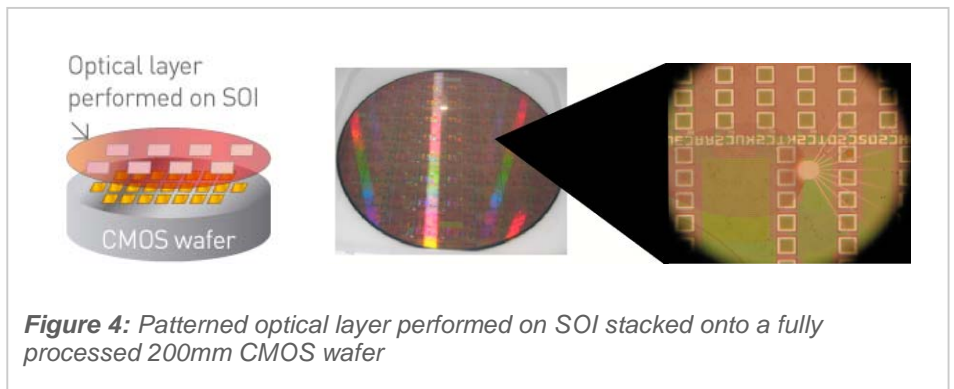
The Smart Stacking technology is adaptable across a range of starting materials as in the example of an RF product built on SOI then transferred to a silica handle wafer with a high dielectric constant. This results in dramatic RF performance improvement to >60GHz with reduced substrate loss and crosstalk, and shown in *Figure 5*.

The Smart Stacking technology has also been applied successfully to resolve obstacles to scaling faced by image sensor manufacturers through exposing the back side of the die. In traditional front-side-illuminated image sensors the photodiode quantum efficiency (QE) has been suffering with

attempts to decrease pixel size and add an increasing number of metal layers and image processing circuits at each pixel.

By using the Smart Stacking technology light can now be detected through the back side of the sensor with significantly higher QE than with the front-side method. This new structure has enabled renewed progress in scaling, and removed metal interconnect density constraints since light no longer needs to pass through the metal to reach the detector (*Figure 6*). The industry has now identified back-side-illuminated (BSI) image sensors as the primary path to continue increasing pixel density, resolution and speed without sacrificing QE.

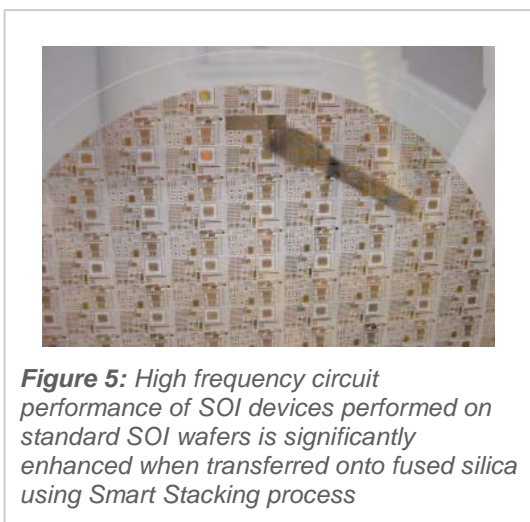
The Smart Stacking process is applied following image sensor fabrication, as shown in *Figure 1*. The processed wafer is molecularly bonded to a handle wafer and the original substrate is thinned down leaving only a few microns of silicon to expose the photodiodes. This maximizes exposure to light and results in a very high QE.



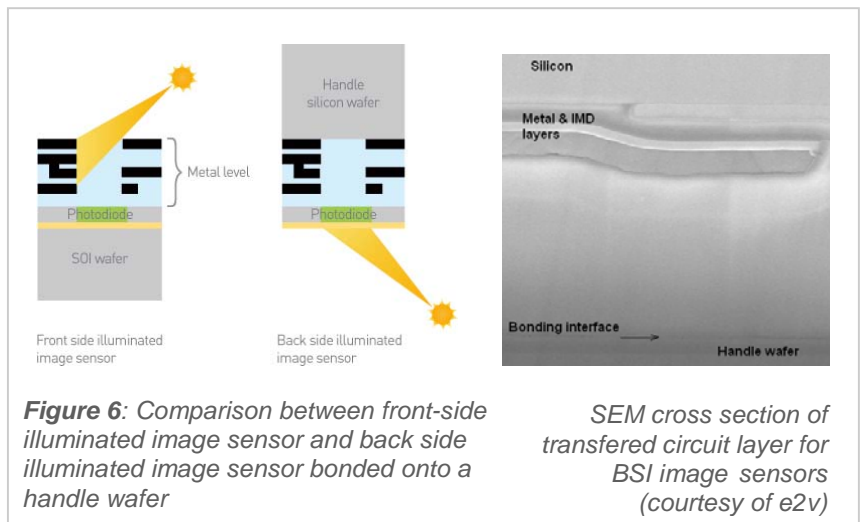
**Figure 4:** Patterned optical layer performed on SOI stacked onto a fully processed 200mm CMOS wafer

Direct low-temperature molecular wafer bonding is best for back-side illuminated applications compared to other bonding options, since it is low stress bonding, minimizing active layer deformation. This is especially critical for BSI image sensors where a fine lithography is performed after the bonding and thinning processes for color filter processing.

If SOI wafers are initially used to fabricate the image sensors then the overall process becomes even more robust. The buried oxide of the SOI wafer acts as a built-in etch stop during the substrate removal process and structurally protects the active silicon layer of the photodiodes during handling. Moreover the almost perfect oxide / silicon interface allows for simplification or elimination of the passivation steps. Color filters and lenses can then be performed onto the backside surface, completing the wafer manufacturing flow.



**Figure 5:** High frequency circuit performance of SOI devices performed on standard SOI wafers is significantly enhanced when transferred onto fused silica using Smart Stacking process



**Figure 6:** Comparison between front-side illuminated image sensor and back side illuminated image sensor bonded onto a handle wafer

SEM cross section of transferred circuit layer for BSI image sensors (courtesy of e2v)

## The Solution

Collaborative partnerships are essential for adopters of new technology to accelerate time-to-market and manage risks. Soitec is a trusted manufacturing and innovation partner to the world's leading electronics companies. The commercial benefits of wafer-to-wafer stacking and 3D integration are significant, and the Smart Stacking building block technologies are available and proven. Breakthrough multi-layer products are possible and already beginning to appear in the marketplace, so now is the best time to explore what the Smart Stacking technology can do for your products.

The Smart Stacking technology is available as a service, with on-demand manufacturing capacity available at Soitec. For each new design a customized process flow is developed based upon the type and quality of starting materials and post-processing requirements. Soitec's expertise, IP and know-how are applied to specific customer application needs to produce solutions that minimize development time, cost and risk.

As the product becomes successful in the marketplace and moves into mass production, Soitec stands ready to license and transfer Smart Stacking technology to our customer's manufacturing line to enable cycle time, cost and material flow optimization. In these cases Soitec continues to be available to its licensees as a second source or as virtual manufacturing capacity available when needed, and stands ready to assist with follow-on product needs.

The Smart Stacking technology platform will grow and expand over time as new solutions and material combinations are proven.

## About Soitec

The Soitec Group is the world's leading innovator and provider of the engineered substrate solutions that serve as the foundation for today's most advanced microelectronic products. The group leverages its proprietary Smart Cut™ technology to engineer new substrate solutions, such as silicon-on-insulator (SOI) wafers, which became the first high-volume application for this proprietary technology. Since then, SOI has emerged as the material platform of the future, enabling the production of higher performing, faster chips that consume less power.

Today, Soitec produces more than 80 percent of the world's SOI wafers. Headquartered in Bernin, France, with two high-volume fabs on-site, Soitec has offices throughout the United States, Japan and Taiwan, and a new production site in Singapore.

Two other divisions, Picogiga International (Les Ulis) and Tracit Technologies (Bernin), complete the Soitec Group. Picogiga delivers advanced substrates solutions, including III-V epiwafers and gallium nitride (GaN) wafers, to the compound material world for the manufacture of high-frequency electronics and other optoelectronic devices. Tracit, on the other hand, provides thin-film layer transfer technologies used to manufacture advanced substrates for power ICs and microsystems, as well as Smart Stacking™, its generic circuit transfer technology for applications such as image sensors and 3D-integration. Shares of the Soitec Group are listed on Euronext Paris. For more information, visit [www.soitec.com](http://www.soitec.com).

*Soitec, Smart Cut, UNIBOND and Smart Stacking are trademarks of S.O.I.TEC Silicon On Insulator Technologies.*

## Customer contacts:

### **Soitec SA (Head Office)**

Parc Technologique des Fontaines  
38190 Bernin  
France

Tel: +33 (0)4 76 92 75 00  
Fax: +33 (0)4 76 92 75 01  
e-mail: [sales@soitec.fr](mailto:sales@soitec.fr)

### **Soitec USA Inc.**

2 Centennial Drive  
Peabody, MA 01960  
USA

Tel: +1-978-531-2222  
Fax: +1-978-278-0075  
e-mail: [soi@soitecusa.com](mailto:soi@soitecusa.com)

### **Soitec Asia Inc.**

Shin-Tokyo Bldg., 3-1, Marunouchi 3-chome,  
Chiyoda-ku, 100-0005, Tokyo  
Japan

Tel: +81-3-5221-7120  
Fax: +81-3-5221-7124  
e-mail: [soitecasia@soitec.com](mailto:soitecasia@soitec.com)

### **Soitec SE Asia**

9F, #289, Xi-Yuan Rd., Xin-Dian City,  
Taipei County, Taiwan, R.O.C.

Tel: +886-972-175-516  
Fax: +886-2-8218-0043  
e-mail: [bill.chu@soitec.com](mailto:bill.chu@soitec.com)

## Press contacts:

### **Company Contact**

Camille Darnaud-Dufour  
International Communications  
The Soitec Group

Mob: (France): +33 (0)6 79 49 51 43  
e-mail: [camille.darnaud-dufour@soitec.com](mailto:camille.darnaud-dufour@soitec.com)