Strained Silicon on Insulator

A quick guide to the technology, the processes, the products

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Staying on Moore's curve by enhancing materials

As the semiconductor industry is moving to more advanced technology nodes, simple scaling of device dimensions and voltages, which worked so well for many decades, is no longer sufficient to continue improving circuit performance. New materials are being introduced and the existing ones are modified to optimize their properties. High dielectric constant (high k) insulators are being developed as an alternative to ultrathin SiO_2 for application as gate insulators. Metal gates or FUSI (fully silicided gates) are expected to replace polysilicon in order to eliminate charge depletion in the gate conductor and provide new options for tuning the threshold voltage Vt. To keep increasing transistor drain currents that largely influence the switching speed of electronic circuits, it is necessary to enhance the flow of electric charges in the transistor channels. Charge mobility is a measure of the velocity of the electrons or holes in the MOS transistor channel.

One solution to increased charge mobility is to use materials other than silicon, for example GaAs or InP. However, these materials lack the level of maturity needed for complex high-density circuits in large volume manufacturing. Another, much more practical solution is to modify the properties of silicon. Strain in silicon can provide significant enhancement to charge mobility. The basic concepts were developed over 20 years ago, but only in the last few years, starting at the 90nm device generation, has it become necessary to use these enhancements.

Process-induced stress in transistor channels is one solution that has worked well at the 90 and 65 nm technology nodes. Uniaxial stress is intentionally applied to transistor channels during device fabrication, tensile for NMOS and compressive for PMOS. This modifies the electronic band structure in silicon in such a way as to improve the carrier mobility. Tensile nitride films are placed over NFETs, while a compressive strain in PFETs is created by a combination of compressive nitride films and SiGe layers that are embedded in the source and drain regions.

As we proceed to the 45nm technology and beyond, process induced stressors, although useful, are no longer sufficient to guarantee the required performance. It is here that the substrate level biaxial tensile strain becomes a platform of choice for building high performance devices.

What is Strained Silicon on Insulator?

Strained silicon on insulator (strained SOI) refers to an engineered composite wafer substrate that chipmakers can use as the starting material for fabricating integrated circuits (ICs). It is the substrate of choice for the upcoming generation of 45nm devices and beyond, especially for high-speed circuits, wireless and broadband communication applications. As such, wafers based on strained silicon on insulator technology are now integrated into the industry's official "roadmap", the International Technology Roadmap for Semiconductors (ITRS).

Strained SOI usually combines two high-performance technological solutions: strained silicon and ultra-thin SOI. However, thicker strained SOI that is suitable for partially depleted (PD) applications is also available.

The advantage of strained silicon lies in its electrical properties. The crystalline lattice of the top,

electrically active layer of silicon is strained so that electric charges (electrons and holes) flow faster. The result is at least a 20- to 50-percent increase in transistor performance.

In SOI, a layer of insulation is introduced between the top face of the silicon wafer, where the chips are fabricated, and the supporting base silicon. The layer of insulation enables the SOI-based chips to function at significantly higher speeds while reducing electrical losses. The result is an increase in performance and a reduction in power consumption.

Together, strained silicon and SOI are key enablers for the industry's move to the upcoming generation of 45nm devices, and will extend to subsequent device generations.

The production of strained SOI substrates requires growing epitaxial SiGe and Si layers, combined with wafer bonding and layer transfer to a handle wafer. A more detailed explanation of the products and processes follows in this paper.

A note about nomenclature: sSOI and SGOI

The first generation of strained SOI that was demonstrated in research papers contained a template layer of fully relaxed SiGe. In keeping with the ITRS nomenclature, this paper refers to this type of strained silicon on insulator as SGOI.

More attractive for commercial applications is the second generation of strained silicon, in which strained Si is placed directly on insulator – without the SiGe template. We refer to this more advanced and more practical generation as sSOI (strained Si On Insulator). It is also known by another name, SSDOI (Strained Si Directly On Insulator).

Soitec's sSOI wafers for high-mobility CMOS applications are sold under the trade name HM Unibond™.

The strain and the challenges

Fabricating strained SOI requires expertise in both strained silicon epitaxy and ultra-thin SOI.

The basic reason for intentionally inducing the strain is as follows. In strained silicon, the spacing between the atoms in the plane of the wafer is greater than it is for regular silicon. This biaxial distortion of the crystal lattice changes the electronic band structure in such a way that it improves electron and hole mobility by up to 70-80%, meaning that electrons and holes move faster through the circuit, resulting in improved performance.

Introducing the strain into the silicon—essentially stretching it in a horizontal plane – requires several Si and SiGe epitaxial steps to obtain the thin layer of strained silicon at the wafer surface.

Soitec, with technical help from some commercial partners, created the industry's first high-volume, production-worthy strained silicon on insulator substrate solutions.

The biaxial strain solution provided by sSOI is the key material for solving the integration issues raised at 45nm and below. Combining the advantages of SOI and strained silicon is the way to minimize process complexity, while achieving the performance gain in keeping with Moore's Law and the low power consumption requirements of the mobile age.

Substrates incorporating 20% germanium in a template layer are today commercially available with dislocation densities below 10^5 cm^{-2} (typical values are about 10^4 cm^{-2}) and with uniformly strained Si films that can be as thin as 15nm or as thick as 90nm.

Soitec is the world's leading manufacturer and supplier of SOI and other engineered wafer substrates. The company holds the patents covering the Smart Cut™ technology, the industry's de facto standard for layer transfer and wafer bonding. In the course of fabricating strained silicon on insulator wafer substrates, bonding and layer transfer to an insulated handle substrate follows the epitaxial steps. Throughout the transfer and bonding, the strain must be preserved. These steps are the domain of the Smart Cut™ technology.

Creating the strain

Epitaxy is growing single crystalline layers on a single crystalline substrate. Atoms being deposited arrange themselves, if the conditions are right, to match the template below. Without a template, the structure would be either polycrystalline (many little randomly oriented crystals) or amorphous (atoms arranged randomly).

Crystalline Ge and crystalline Si have the same lattice structure, so in theory a silicon lattice can be aligned on a germanium template. However, germanium atoms are bigger, and the spacing between them is 4.2% greater than the spacing between silicon atoms (that is, silicon and germanium have different lattice constants). If one could epitaxially deposit the silicon over the germanium and get the silicon lattice to align with the germanium lattice, the result would be silicon with about 4% strain. But in practice, the difference in lattice constants between pure germanium and pure silicon is too great, the silicon lattice stretches, but the lattices don't line up perfectly, resulting in many crystalline defects, such as misfit and threading dislocations.

SiGe alloys have a lattice constant that is in-between those of silicon and germanium and can be varied by adjusting the ratio of Si to Ge. When a thin layer of pure silicon is grown on SiGe, the silicon atoms try to align themselves with the SiGe atoms below. The result is that the atoms in the silicon layer are spaced further apart in the horizontal plane than they would be otherwise – here is the strain: the thin layer of Si is stretched like a rubber membrane as it tries to conform to SiGe in the template below.

But even getting a high quality SiGe template is tricky. An abrupt change from a Si substrate to a Ge-rich layer is likely to cause excessive densities of threading dislocations and other defects in SiGe and in the final strained silicon lattice structure.

Instead, the strategy often is to epitaxially grow a stack of layers that begins with a "buffer" layer of Si and Ge on bulk silicon. In the buffer layer, the fraction of germanium typically starts at zero at the bottom and goes up to the final value of 20% at the top (or possibly 40% in future products). See Figure 1. Other types of buffer layers are also possible.

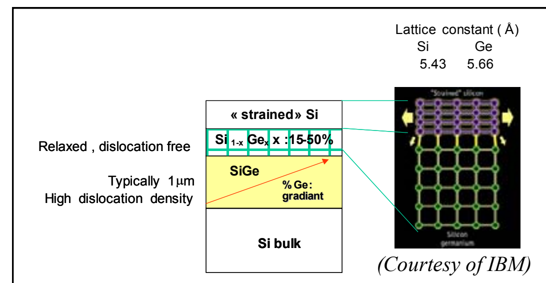

Figure 1. Straining silicon requires several epitaxial steps: a SiGe buffer on bulk Si; a relaxed SiGe template on the buffer SiGe; and Si on the relaxed SiGe template, which strains this top layer of silicon.

Over the top of the buffer layer, another "template" layer is grown; its lattice constant matches the top of the buffer layer. This template layer has a uniform amount of SiGe throughout: enough germanium to get a lattice constant sufficient to stretch the final cap layer of silicon, but not enough to introduce large numbers of defects. There is no strain in the template layer, so it is referred to as "relaxed". If the SiGe layer is fully relaxed, the cap layer of silicon deposited on it will then be optimally strained.

Layer transfer

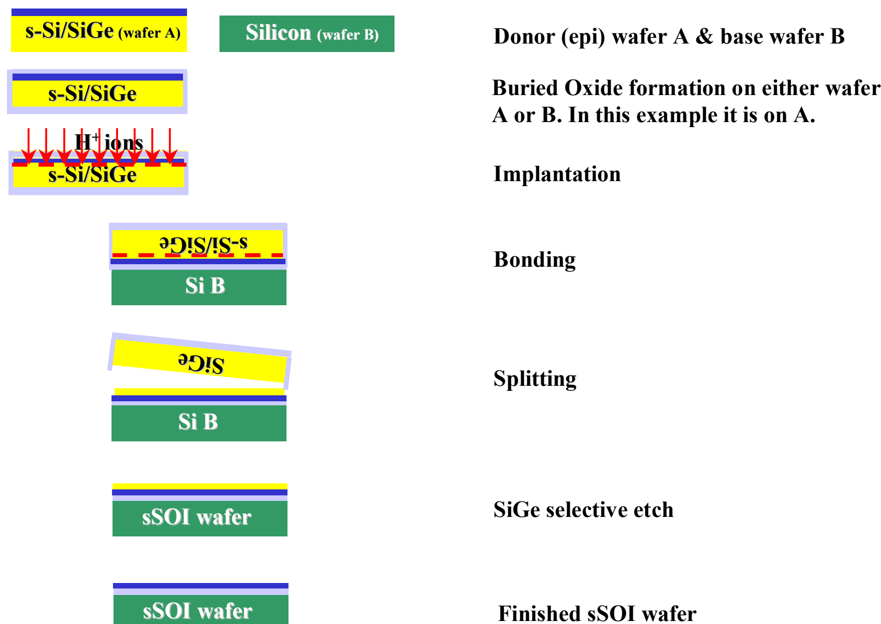

Figure 2: sSOI fabrication process flow.

sSOI fabrication strategies

Strained silicon on insulator (sSOI) consists of a layer of strained silicon bonded directly onto another wafer in such a way that there is a layer of silicon dioxide between the strained Si film and a handle wafer. The process is designed to be as similar as possible to the method of fabricating conventional SOI wafers. Just like in SOI, the bond interface is usually placed near the handle wafer. Strained Si films, typically about 200 Å thick, are transferred directly to a new handle wafer, followed by removal of the residual SiGe layer by selective etching. Such thin films are most suited for fully depleted device architectures. Thicker strained silicon films, up to 900Å, are also available. Both types of films are fully stable under all typical thermal processing steps used in CMOS fabrication, even at 1100°C. The fact that the strained Si is supported by amorphous insulator and not by a SiGe template eliminates most of nucleation sites for relaxation and improves the strain stability.

Since sSOI has the same basic structure as conventional SOI, the actual film thicknesses for sSOI devices is similar to the guidelines that the industry's roadmap indicates for conventional SOI. Nevertheless, to fully optimize device performance it is important to consider the modified mobility values, shifts in threshold voltages Vt induced by the modified band structure of silicon, and slight changes in diffusion rates of some dopants.

sSOI use is expected in high performance logic applications for the 45nm technology node and below. While SiGe is used in interim sSOI fabrication steps, once the requisite strain is established in the silicon cap layer, the SiGe is removed by layer transfer and selective etchback. The fabrication strategy for high-volume sSOI production has been established and demonstrated in practice.

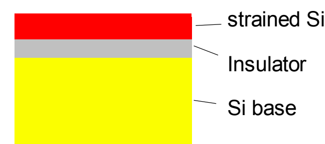

Figure 3. In sSOI, the strained Si is bonded directly to the insulating layer.

sSOI in state-of-the-art devices: strain hybridization

Since conventional device scaling is no longer possible, it is necessary to use every possible method to produce the necessary enhancements. Currently this means utilizing *both* the substrate level biaxial tensile strain *and* the device level uniaxial strain.

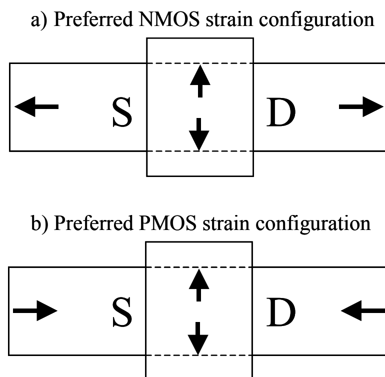

Figure 4. Ideal strain configurations for NMOS and PMOS are shown schematically in (a) and (b).

Figure 4 shows the preferred strain configurations for NMOS and PMOS. In an NMOS device (4a), biaxial tensile strain as provided in sSOI is shown. This enhances current drive. Any additional process-induced uniaxial tensile strain can be superimposed on the substrate level strain for even greater performance boost. This is demonstrated in data from Freescale in Figure 5, where adding uniaxial strain to conventional SOI increases drive current by 9% but adding the same tensile etch stop layer (tESL) to sSOI gives a total boost of 9%+18% as compared to SOI alone. In other words, everything else being equal, sSOI improves the current by 18%.

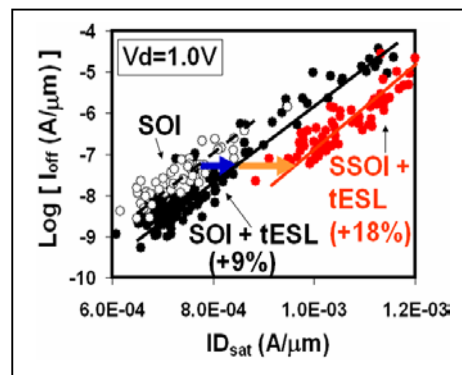

Figure 5. Drive current ID_{sat} vs. I_{off} for NMOS devices with various stressors. (A. Thean et al., VLSI 2006).

Figure 4(b) shows the ideal strain configuration for PMOS as determined from piezoelectric coefficients of silicon – uniaxial compression along the current flow and tension in the direction normal to it. This configuration cannot be obtained by either substrate level or process-induced strain alone. Compression along the current flow axis can be produced by strained nitride etch stop layers and/or by SiGe epitaxial layers embedded in the source/drain regions. STI (shallow trench isolation) can produce compression along one or both lateral axes, depending on device geometry.

However, to obtain the desired configuration as shown in Figure 4(b), it is necessary to combine an sSOI substrate with process-induced strain, for example with cESL. For best results, during device processing on sSOI an additional step of Selective Uniaxial Relaxation (SUR) is implemented to eliminate tensile strain parallel to the device axis, while preserving the transverse tensile strain.

Subsequently, conventional uniaxial compressive stressors are applied. The finished PMOS devices have the most desired configuration (Figure 4 (b)) with uniaxial tension perpendicular to the current, and uniaxial compression along the current.

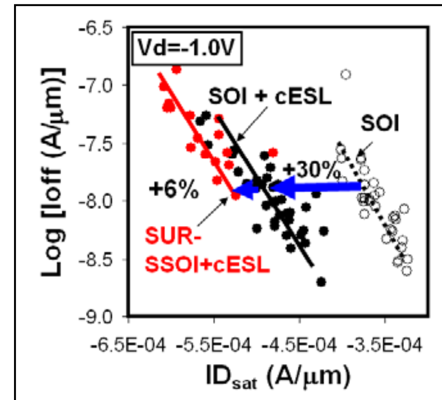

Figure 6. Drive current ID_{sat} vs. I_{off} for PMOS devices with various stressors. (A. Thean et al., VLSI 2006).

Data in Figure 6 show that cESL alone improves ID_{sat} by 30%, but sSOI with SUR adds another 6%. Further optimization is expected to yield much greater enhancements.

To summarize, by combining uniaxial stressors with a biaxially tensile starting sSOI substrate, both NMOS and PMOS devices are improved beyond what would be possible with process-induced strain alone.

Future perspectives

sSOI wafers with built-in strain of about 0.8% (stress of about 1.3 GPa) that are based on Si epitaxy on 20% Ge SiGe are now a commercial reality. Such wafers have a threading dislocation density on the order of 10^4 cm^{-2} and no dislocations pile-ups (which had been a significant problem during the early days of strained Si). This level of strain is especially useful for NMOS. While it provides less enhancement for PMOS, PMOS devices can be further enhanced using strain hybridization with process-induced stressors.

To improve hole mobility in PMOS with substrate-level strain alone, it is necessary to increase the biaxial strain to about 1.5% (stress of 2.5-3 GPa). Relaxed layers of SiGe with 40% Ge need to be grown as virtual substrates for strained Si epitaxy. Such highly strained films have been demonstrated but significant optimization is still required to reduce defect densities.

Another very exciting aspect of sSOI substrates is that they provide an excellent platform for the future dual-channel devices. Compressive SiGe locally grown on tensile Si can lead to extremely high hole mobilities in PFETs, while NFETs would continue to take advantage of biaxially tensile Si alone.

About Soitec

The Soitec Group is the world's leading innovator and provider of the engineered substrates that serve as the foundation for today's most advanced electronic products and nanotechnologies. Headquartered in Bernin, France, the company manufactures its comprehensive portfolio of engineered substrates, including silicon-on-insulator (SOI) and strained SOI (sSOI), using Soitec's proprietary Smart Cut™ technology—the de facto industry standard. With its strong global presence, patented technology and industry-leading production capacity, Soitec is helping to drive the performance and power advantages that are key to the smaller, more power efficient, and increasingly mobile electronic products favored by consumers worldwide. Both shares and convertible bonds are listed on Euronext Paris. Additional information is available at www.soitec.com.

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